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WHAT IS CLAIMED IS:

1. An array substrate for a liquid crystal display device, which has thin film transistors (TFTs), gate lines including even numbered gate lines and add numbered gate lines, gate pads, data lines and data pads on a substrate, comprising:

a first gate shorting bar disposed substantially perpendicular to the gate lines in a peripheral portion of the substrate;

a second gate shorting bar spaced apart from and substantially parallel with the first gate shorting bar;

a plurality of pixel electrodes, each pixel electrode contacting a respective one of the thin film transistors; and

a connecting line connecting the first shorting bar to the even numbered gate lines and including a first line portion and a second line portion;

wherein the first line portion is separated into two part; and wherein the second line portion has a neck shaped bridge portion at one time during a fabrication process and then separated into two parts.

2. The array substrate according to claim 1, wherein the Mo-Bridge has a width in the range of about 3.5 to about 4.5 micrometers, a length in the range of about 2 to about 8 micrometers and first and second slanting portions in a chevron pattern.

3. The array substrate according to claim 2, wherein the first slanting portion forms an angle in the range of about 20 to about 70 degrees and the second slanting portion forms an angle in the range of about 110 to about 160 degrees with a line substantially parallel with the connecting line.

4. The array substrate according to claim 1, wherein the said second line portion is separated into two parts by a distance of less than about 5 micrometers.

5. The array substrate according to claim 1, wherein the second line portion of the connecting line is formed of molybdenum (Mo).

6. The array substrate according to claim 1, wherein the first line portion of the connecting line includes at least aluminum (Al).

7. The array substrate according to claim 1, wherein the first line portion of the connecting line is formed of aluminum neodymium (AlNd).

8. The array substrate according to claim 1, further comprising a gate insulation layer on the connecting line and a passivation layer on the thin film transistors.

9. The array substrate according to claim 1, wherein the plurality of pixel electrodes are formed of a transparent material selected from a group consisting of indium tin oxide and indium zinc oxide.

10. The array substrate according to claim 1, wherein each thin film transistor includes a double-layered gate electrode.

11. A method of fabricating an array substrate for a liquid crystal display device, comprising the steps of:

forming a first metal layer on a substrate;

forming a second metal layer on the first metal layer;

patterning the first and second metal layers to form connecting lines including a bridge portion in the patterned second metal layer and to form a plurality of gate electrodes, gate lines, gate pads, shorting bars;

forming a gate insulation layer on the substrate to cover the patterned first and second metal layers;

forming an active layer and an ohmic contact layer over each gate electrode;

removing a portion of the gate insulation layer disposed on the bridge portion and a portion of first layer of the connecting line under the bridge portion;

forming a third metal layer on the gate insulation layer and on the bridge portion;

patterning the third metal layer so as to form a plurality of source electrodes and drain electrodes;

eliminating the bridge portions when patterning the third metal layer; and

forming a passivation layer on the gate insulation layer, on the connecting line and on the patterned third metal layer.

12. The method of fabricating an array substrate according to claim 11, wherein each bridge portion has a width in the range of about 3.5 to about 4.5 micrometers and a length in the range of about 2 to about 8 micrometers.

13. The method of fabricating an array substrate according to claim 11, further comprising:

patterning the passivation layer so as to form a plurality of drain contact holes; and

forming a plurality of pixel electrodes that contact respective drain electrodes through the drain contact holes.

14. The method of fabricating an array substrate according to claim 13, wherein the plurality of pixel electrodes are formed of a transparent material selected from a group consisting of indium tin oxide and indium zinc oxide.

15. The method of fabricating an array substrate according to claim 11, wherein the first metal layer includes at least aluminum.

16. The method of fabricating an array substrate according to claim 11, wherein the first metal layer is aluminum neodymium.

17. The method of fabricating an array substrate according to claim 11, wherein the second metal layer and third metal layer are molybdenum.

18. The method of fabricating an array substrate according to claim 11, wherein each bridge portion has a neck shape including first and second slanting portions.

19. The method of fabricating an array substrate according to claim 18, wherein the first slanting portion forms an angle in the range of about 20 to about 70 degrees with a line substantially parallel with the connecting line.

20. The method of fabricating an array substrate according to claim 18, wherein the second slanting portion forms an angle in the range of about 110 to about 160 degrees with a line substantially parallel with the connecting line.

21. The method of fabricating an array substrate according to claim 11, wherein the first layer of the connecting lines is separated into two parts by a distance of less than about 5 micrometers.

22. The method of fabricating an array substrate according to claim 11, wherein each gate electrode consists of two layers.

23. The method of fabricating an array substrate according to claim 22, wherein the first layer of the gate electrode is aluminum and the second layer of the gate electrode is molybdenum.

24. A method of fabricating an array substrate for a liquid crystal display device, comprising the steps of:

forming a buffer layer on a substrate;

forming a polycrystalline-silicon active layer on the buffer layer, the said active layer having an island shape;

forming a gate insulation layer on the buffer layer to cover the polycrystalline-silicon active layer;

forming a first metal layer on the gate insulation layer;

forming a second metal layer on the first metal layer;

patterning the first and second metal layer to form a gate electrode, a gate line and a gate shorting bar;

forming a source contact area and a drain contact area at both sides of the polycrystalline-silicon active layer;

forming an interlayer insulator on the gate insulation layer to cover the patterned first and second metal layers;

patterning the interlayer insulator and the gate insulation layer so as to form a first contact hole to the source contact area and a second contact hole to the drain contact area, patterning a portion of the interlayer insulator on the gate shorting bar so as to form an etching hole, eliminating a portion of the first metal layer of the gate shorting bar under the etching hole, and forming an bridge portion in the second metal layer of the gate shorting bar under the etching hole;

forming a third metal layer on the gate insulation layer and on the bridge portion;

patterning the third metal layer so as to form a source electrode and a drain electrode, and removing the bridge portion when patterning the third metal layer; and

forming a passivation layer on the interlayer insulator and on the patterned third metal layer.

25. The method of fabricating an array substrate according to claim 24, wherein the first metal layer is an aluminum layer having a thickness of about 3000 angstroms.

26. The method of fabricating an array substrate according to claim 24, wherein the second metal layer is a molybdenum layer having a thickness of about 500 angstroms.

27. The method of fabricating an array substrate according to claim 24, wherein the third metal layer is a molybdenum layer having a thickness of about 500 angstroms.

28. The method of fabricating an array substrate according to claim 24, wherein the interlayer insulator is made of silicon nitride and has a thickness of about 7000 angstroms.

29. The method of fabricating an array substrate according to claim 24, wherein the bridge portion has a neck shape.

30. The method of fabricating an array substrate according to claim 29, wherein the neck-shaped bridge portion has a width of about 4 micrometers.

31. The method of fabricating an array substrate according to claim 29, wherein the neck-shaped bridge portion has a slanting portion.

32. The method of fabricating an array substrate according to claim 31, wherein the slanting portion forms an angle in the range of about 20 to about 70 degrees with a line substantially perpendicular to the gate shorting bar.

33. The method of fabricating an array substrate according to claim 29, wherein the neck-shaped bridge portion has a length in the range of about 2 to about 8 micrometers.

34. The method of fabricating an array substrate according to claim 24, wherein the gate insulation layer is formed of an insulating material selected a group consisting of silicon nitride and silicon nitride.

35. The method of fabricating an array substrate according to claim 24, further comprising the steps of:

forming a planar layer on the passivation layer;

pattering the planar layer and the passivation layer so as to form a drain contact hole to the drain electrode;

forming the transparent conductive material on the planar layer; and

patterning the transparent conductive material so as to form a pixel electrode contacting the drain electrode through the drain contact hole.